Analog, RF and EMC Considerations in Printed Wiring Board (PWB) Design

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Telephonics - Command Systems Division
Introduction

♦ Advances in digital and analog technologies present new challenges PWB design

♦ Clock frequencies approach the L Band region
  - Dielectric absorption, Skin Depth, Impedances, Dispersion

♦ High Power and/or Lower Voltage
  - Power distribution, decoupling

♦ High dynamic-range/low-noise analog circuitry
  - Noise immunity, stability

♦ High Density Components
  - Xilinx FG1156 Fine Pitch BGA (1.0 mm pitch 39 mils)
  - Finer pitch BGAs 0.8 mm (31 mils) and 0.5 mm (20 mils)

♦ Overlap between Disciplines
  - Electrical, Mechanical, Manufacturing, Design/Drafting
Outline

♦ PWB Construction
  - Types, Stack-Ups

♦ PWB Materials
  - Core/pre-preg, copper weights

♦ Signal Distribution
  - Impedance, Coupling, Signal Loss, Delay

♦ Power Distribution & Grounding
  - Planes, Decoupling, Power Loss

♦ References and Vendors
PWB Construction
PWB/CCA Examples
Types of Rigid PWB

- Rigid, One Layer, Type 1
- Rigid, Two Layer, Type 2
- Rigid, Multi Layer, w/o blind/buried vias, Type 3
- Rigid, Multi Layer, w/ blind/buried vias, Type 4
- Rigid, Metal Core, w/o blind/buried vias, Type 5
- Rigid, Metal Core, w/ blind/buried vias, Type 6

(Per IPC-2222 standard)
Types of Flex PWB

- Flex, One Layer, Type 1
- Flex, Two Layer, Type 2
- Flex, Multi Layer, Type 3
- Flex, Multi Layer, Rigid/Flex, Type 4

(Per IPC-2223 Standard)
Footnotes on Flex PWBs

♦ Used as alternative to a discrete wiring harness
♦ Many similarities to rigid PWBs
♦ Typically higher development cost than harness
♦ Typically cheaper than harness in production
♦ Improved repeatability
♦ Improved EMI performance and impedance control when ground layers are used
♦ Typically much less real estate needed
PWB Stack-Ups (1 and 2 Layer)

One Sided
- Inexpensive
- Applicable to straightforward circuits
- Difficult to control EMI without external shield
- Difficult to control impedance

Signals, Grounds, Supplies
Dielectric

Two Sided
- Inexpensive (slightly more than 1 sided)
- Applicable to more complex circuits
- EMI mitigation with ground plane
- Impedance control simplified with ground plane

Signals, Ground, Supplies
Dielectric
Ground (Signals, Supplies)
Multi-Layer PWBs

- Option for dedicating layers to ground
  - Forms reference planes for signals
  - EMI Control
  - Simpler impedance control

- Option for dedicating layers to Supply Voltages
  - Low ESL/ESR power distribution

- More routing resources for signals
Exploded View of Multi-Layer PWB

- **Core Construction**
  - As shown

- **Foil Construction**
  - Reverse core and pre-preg
Multi-Layer Stack-Up Examples

1. High Speed Digital PWB
   - High Density
   - Ten Layers
   - Two Micro-Strip Routing Layers
   - Four Asymmetrical Strip-Line Routing Layers
   - Single Supply Plane
   - Two Sided

2. High Speed Digital PWB
   - Moderate Density
   - Six Layers
   - Two Micro-Strip Routing Layers
   - Two Buried Micro-Strip Routing Layers
   - Single Supply Plane
   - Two Sided

3. Mixed Analog/RF/Digital PWB
   - Moderate Density
   - Ten Layers
   - Two Micro-Strip Routing Layers
   - Four Asymmetrical Strip-Line Routing Layers
   - Single Digital Supply Plane
   - Analog supplies on inner layers
     - Routing Clearance Considerations
     - Improved isolation
   - Two Sided
PWB Stack-Up Guidelines

♦ Maximize symmetry to simply manufacturing and to mitigate warping

♦ Even number of layers preferred by PWB manufacturers

♦ Asymmetrical strip-line has higher routing efficiency than symmetrical strip-line

♦ Supply planes can be used as reference planes for controlled Z (but not preferred for analog)

♦ Ideally, supply planes should be run adjacent to ground planes
PWB Materials
PWB Materials

♦ Dozens of dielectric materials to choose from
  - Rogers 20 types
  - Taconic 10 types
  - Polyclad 25 types
  - Park Nelco 30 types
♦ Several dielectric thickness options
♦ Several copper thickness options
♦ Two copper plating options
  - Rolled
  - Electro-Deposited
Electrical Considerations in Selecting Material

- **Dielectric Constant (permittivity)**
  - The more stable, the better
  - Lower values may be more suitable for high layer counts
  - Higher values may be more suitable for some RF structures

- **Loss Tangent**
  - The lower, the better
  - Becomes more of an issue at higher frequencies

- **Moisture Absorption**
  - The lower, the better
  - Can effect dielectric constant and loss tangent

- **Voltage Breakdown**
  - The higher, the better
  - Typically not an issue, except in high voltage applications

- **Resistivity**
  - The higher, the better
  - Typically not an issue, except in low leakage applications
Mechanical Considerations in Selecting Materials

♦ Peel Strength
  - The higher, the better

♦ Flammability
  - UL Standards

♦ Glass Transition Temperature ($T_g$)

♦ Thermal Conductivity
  - Typically PWB material is considered an insulator
  - Thermal Clad (Bergquist)
  - Planes & vias contribute to thermal conductivity

♦ Coefficient of Expansion
  - XY matching to components, solder joint stress (LCC)
  - Z axis expansion, via stress

♦ Weight (density)

♦ Flexibility
# PWB Material Examples

<table>
<thead>
<tr>
<th>Material</th>
<th>Dielectric Constant ($\varepsilon_r$)</th>
<th>Loss Tangent (tan(\delta))</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>FR-4, Woven Glass/Epoxy</td>
<td>4.7 (1 MHz) 4.3 (1 GHz)</td>
<td>0.030 (1 MHz) 0.020 (1 GHz)</td>
<td>Inexpensive, available, unstable $\varepsilon_r$, high loss</td>
</tr>
<tr>
<td>N7000-1 Polyimide Park-Nelco</td>
<td>3.9 (2.5 GHz) 3.8 (10 GHz)</td>
<td>0.015 (2.5 GHz) 0.016 (10 GHz)</td>
<td>High $T_g$ (260 °C)</td>
</tr>
<tr>
<td>CLTE Arlon</td>
<td>2.94 (10 GHz)</td>
<td>0.0025 (10 GHz)</td>
<td>Stable $\varepsilon_r$, low loss</td>
</tr>
<tr>
<td>RT6010LM Rogers</td>
<td>10.2 (10 GHz)</td>
<td>0.002 (10 GHz)</td>
<td>High $\varepsilon_r$, high loss</td>
</tr>
<tr>
<td>RO4350B Rogers</td>
<td>3.48 (10 GHz)</td>
<td>0.004 (10 GHz)</td>
<td>Stable $\varepsilon_r$, low loss, processing is similar to FR4</td>
</tr>
<tr>
<td>RT6002 Rogers</td>
<td>2.94 (10 GHz)</td>
<td>0.0012 (10 GHz)</td>
<td>Stable and accurate $\varepsilon_r$, low loss</td>
</tr>
</tbody>
</table>
Dielectric, Common Thickness

♦ Core Material
- 0.002, 0.003, 0.004, 0.005, 0.006, 0.007, 0.008, 0.009
- 0.010, 0.012, 0.014, 0.015, 0.018, 0.020, 0.031

♦ Pre-Preg
- 0.002, 0.003, 0.004, 0.005, 0.008
- Pre-preg can be stacked for thicker layers

♦ Use standard thickness in designing stack-up

♦ Work with anticipated PWB vendor(s) when assigning stack-up and selecting material
Copper Options

♦ Common Thickness Options

<table>
<thead>
<tr>
<th>Weight</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25 oz</td>
<td>0.4 mil (9 µm)</td>
</tr>
<tr>
<td>0.5 oz</td>
<td>0.7 mil (18 µm)</td>
</tr>
<tr>
<td>1.0 oz</td>
<td>1.4 mil (35 µm)</td>
</tr>
<tr>
<td>2.0 oz</td>
<td>2.8 mil (70 µm)</td>
</tr>
</tbody>
</table>

♦ Plating Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Surface Roughness</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rolled</td>
<td>55 µ in</td>
<td>Lower loss at high frequency (&gt;1 GHz)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>More precise geometries for critical applications (couplers, distributed filters)</td>
</tr>
<tr>
<td>Electro Deposited</td>
<td>75 µ in (0.5 oz)</td>
<td>For Treated (Dendritic) Side</td>
</tr>
<tr>
<td></td>
<td>94 µ in (1 oz)</td>
<td>Untreated (Drum) Side is 55 µ in</td>
</tr>
<tr>
<td></td>
<td>120 µ in (2 oz)</td>
<td>Less prone to pealing</td>
</tr>
</tbody>
</table>

Electro Deposited copper has a “Drum” side and “Treated” side.
Considerations in Selecting Copper Thickness & Plating

♦ Power Handling
  - Current capacity and temperature rise
  - Trace failure due to short

♦ Loss
  - Thicker/wider lines reduce DC resistive loss
  - Rolled copper exhibits less loss (>1 GHz)

♦ Etch-Back
Etch-Back

♦ Actual trace shape is trapezoidal
♦ Thinner copper produces more precise geometries with narrow line widths
♦ For traces >5 mils, 1 oz is acceptable
♦ For traces <5 mils, thinner copper used to limit etch-back
♦ Guidelines are vendor dependant
Etch-Back

♦ Critical in some RF applications
  - Directional Couplers, Distributed Filters

♦ Critical in some narrow line width geometries
  - Significantly effects current capacity of trace
  - Significantly effects trace resistance and loss

♦ In many applications, effects on $Z_0$, L, C can be ignored (Buried Micro-Strip Example)

<table>
<thead>
<tr>
<th>$\theta$</th>
<th>L(nH/in)</th>
<th>C(pF/in)</th>
<th>$Z_0$ (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>90</td>
<td>8.5</td>
<td>3.4</td>
<td>50.0</td>
</tr>
<tr>
<td>79</td>
<td>8.6</td>
<td>3.3</td>
<td>50.7</td>
</tr>
<tr>
<td>72</td>
<td>8.6</td>
<td>3.3</td>
<td>51.0</td>
</tr>
<tr>
<td>60</td>
<td>8.7</td>
<td>3.3</td>
<td>51.5</td>
</tr>
<tr>
<td>45</td>
<td>8.8</td>
<td>3.2</td>
<td>52.2</td>
</tr>
</tbody>
</table>
Signal Distribution
Single Ended Structure Examples

- Micro-Strip: Signal Trace, Ground Plane, Dielectric, W, t, h
- Buried Micro-Strip
- Asymmetrical Strip-Line
- Symmetrical Strip-Line
Single Ended Structure Examples
(continued)

Surface Coplanar Waveguide

Embedded Coplanar Waveguide

Surface Coplanar Waveguide with Ground Plane

Embedded Coplanar Waveguide with Ground Plane
Differential Structure Examples

Edge Coupled

- Edge-Coupled Micro-Strip
- Edge-Coupled Asymmetrical Strip-Line
- Edge-Coupled Symmetrical Strip-Line

Broadside Coupled

- Edge-Coupled Imbedded Micro-Strip
- Broadside-Coupled Strip-Line
- Offset Broadside-Coupled Strip-Line
PWB traces as Transmission Lines

- Signal wavelength approaches component size
- Dielectric Loss (G)
- Trace Copper Loss (R)
- Trace series inductance (L)
- Trace capacitance (C)
Characteristic Impedance

\[ Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \]  
Line impedance in terms of R, L, C and G

\[ Z_0 = \sqrt{\frac{L}{C}} \]  
Line Impedance for Lossless line (R and G \to 0)
Trace Impedance

- Impedance Determined By
  - Topology
  - Dielectric constant of PWB material
  - Dielectric height
  - Conductor width
  - Conductor thickness (small extent)

- Impedance Critical
  - Delivering max power to load
  - Maintaining signal integrity
  - Prevent excessive driver loading
Strip-Line & Micro-Strip Impedance

Micro-Strip

Strip-Line

\[ Z_0 = \frac{87}{\sqrt{\varepsilon_r} + 1.41} \ln \left( \frac{5.98h}{0.8w + t} \right) \]

when \( \frac{w}{h} < 2.0 \) and \( 1 < \varepsilon_r < 15 \)

\[ Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln \left( \frac{1.9b}{0.8w + t} \right) \]

when \( \frac{w}{h} < 0.35 \) and \( \frac{t}{h} < 0.25 \)
Asymmetrical Strip-Line Impedance

\[ Z_0 = \sqrt{\frac{\mu_0}{\varepsilon_0}} \cosh^{-1} \left[ \sin \left( \frac{\pi (b-s)}{2b} \right) \coth \left( \frac{\pi d_0}{2b} \right) \right] \]

\[ d_0 = w \left( 0.5008 + 1.0235 \left( \frac{t}{w} \right) - 1.0230 \left( \frac{t}{w} \right)^2 + 1.1564 \left( \frac{t}{w} \right)^3 - 0.4749 \left( \frac{t}{w} \right)^4 \right) \]

when \( \frac{w}{b-t} < 0.35 \)
Impedance Examples

♦ Symmetrical Strip-Line
50 Ω, 11 mils wide
(30 mil dielectric)

♦ Asymmetrical Strip-Line
50 Ω, 9 mils wide
(10+20=30 mil dielectric)

♦ Micro-Strip
50 Ω Micro-Strip, 54 mils wide
(30 mil dielectric)

Notes:
1. Copper: 1 oz, electro-deposited
2. FR4 dielectric constant: 4.50
Loss

♦ Loss due to three components
  - Dielectric Loss (loss tangent of PWB material)
  - Conductor Loss (resistive, skin effect, roughness)
  - Radiation Loss (typically negligible)

♦ Loss in Digital Applications
  - High Speed
  - Long Trace Runs
  - and/or Fine Width Lines

♦ Loss in Analog/RF Applications
  - Gain/Loss budgets in RF and IF paths
  - LO distribution loss
  - Scaling in Video, ADC or DAC applications
## Dielectric and Copper Loss Examples

<table>
<thead>
<tr>
<th>Frequency</th>
<th>FR4</th>
<th></th>
<th></th>
<th>4350</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Copper Loss</td>
<td>Dielectric Loss</td>
<td>Total Loss</td>
<td>Copper Loss</td>
<td>Dielectric Loss</td>
<td>Total Loss</td>
</tr>
<tr>
<td>10 MHz</td>
<td>0.005</td>
<td>0.001</td>
<td>0.006</td>
<td>0.005</td>
<td>0.000</td>
<td>0.005</td>
</tr>
<tr>
<td>100 MHz</td>
<td>0.019</td>
<td>0.012</td>
<td>0.031</td>
<td>0.019</td>
<td>0.002</td>
<td>0.021</td>
</tr>
<tr>
<td>1 GHz</td>
<td>0.090</td>
<td>0.123</td>
<td>0.213</td>
<td>0.090</td>
<td>0.017</td>
<td>0.107</td>
</tr>
<tr>
<td>10 GHz</td>
<td>0.330</td>
<td>1.227</td>
<td>1.557</td>
<td>0.330</td>
<td>0.173</td>
<td>0.503</td>
</tr>
</tbody>
</table>

**FR4 dielectric loss exceeds copper loss at 1 GHz**

**Notes:**
1. Copper: 1 oz, electrodeposited, 10 mil width, 50 Ohms, strip-line
2. FR4 dielectric constant: 4.50, loss tangent 0.025, height 28 mils
3. 4350 dielectric constant: 3.48, loss tangent 0.004, height 22 mils
4. Loss units are dB/inch
Conductor Loss

DC Resistance

\[ R_{DC} = \rho \frac{l}{tw} = \rho \frac{l}{A} \]

\[ R_{DC} = 0.679 \ \mu\Omega \ - \ in \ \frac{12 \ in}{(0.0014 \ in)(0.010 \ in)} = 0.6 \Omega \]

\[ R_{DC} = 0.679 \ \mu\Omega \ - \ in \ \frac{12 \ in}{(0.0007 \ in)(0.005 \ in)} = 2.3 \Omega \]

Skin Depth

\[ \delta = \sqrt{\frac{\rho}{\pi f \mu_0}} \]

\[ \delta = \sqrt{\frac{0.0172 \ \mu\Omega m}{\pi (10 \ GHz) \left( 4\pi \times 10^{-7} \ \Omega \frac{s}{m} \right) \left( 4\pi \times 10^{-7} \ \frac{\Omega \cdot s}{m} \right)}} = 660 \ nm = 0.03 \ mils \]

\[ \delta = \sqrt{\frac{0.0172 \ \mu\Omega m}{\pi (10 \ MHz) \left( 4\pi \times 10^{-7} \ \Omega \frac{s}{m} \right) \left( 4\pi \times 10^{-7} \ \frac{\Omega \cdot s}{m} \right)}} = 21 \ \mu m = 0.8 \ mils \]

• Current density drops to 37% (1/e)
• Ignore if \( t < 2\delta \)
Loss due to Skin Effect & Roughness

Resistance, 5 mil Line
(on 1 oz and 0.5 oz copper)

Loss Variation, Roughness
(1 oz, 11 mil width)
**Time Delay**

\[
 t_d = \sqrt{L_o C_o} = \sqrt{\frac{\varepsilon_{r\text{-effective}}}{c}} = 85\sqrt{\varepsilon_{r\text{-effective}}} \text{ ps/inch}
\]

Where:
- \( t_d \): time delay per unit length
- \( \varepsilon_{r\text{-effective}} \): Effective Relative Dielectric constant
- \( C_o \): Capacitance per unit length
- \( c \): Speed of Light

\[
\varepsilon_{r\text{-effective}} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \left( \frac{1}{\sqrt{1 + \frac{12h}{w}}} \right)
\]

when \( \frac{w}{h} \geq 1 \)

\[
t_d = 156 \text{ ps/inch}
\]

(FR4, \( \varepsilon_r = 4.5 \), \( w = 18\text{mils}, h = 10\text{mils} \))

For strip-line:

\[
\varepsilon_{r\text{-effective}(strip-line)} = \varepsilon_r
\]

\[
t_d = 85\sqrt{\varepsilon_r} \text{ ps per inch}
\]

(FR4, \( \varepsilon_r = 4.5 \))

For micro-strip:

\[
\varepsilon_{r\text{-effective}(micro-strip)} < \varepsilon_{r\text{-effective}(buried micro-strip)} < \varepsilon_r
\]

\[
t_d = 180 \text{ ps/inch}
\]

(FR4, \( \varepsilon_r = 4.5 \))
Signal Dispersion

♦ Frequency Dependant Dielectric Constant
  - Propagation velocity is frequency dependant
  - PWB acts as a dispersive Medium

♦ Becomes Issue
  - Long Trace Runs
  - High Speed Clocks
  - Critical Analog
信号分散

♦ 恒定的时间延迟是必要的，以确保信号在到达目的地时未被失真。
Signal Dispersion Example

- Eye Diagram
- 4.8 Gbps
- 36” trace length

FR4

ROGERS 4350

ARLON CLTE

Er vs Frequency

- FR4
- RO4350

Frequency in MHz

Er 4

3 5

100 1000 2000 10000
Mitigation of Dispersion

- More Stable Dielectric
  - Option for new designs

- Pre-Emphasis Filter
  - Option for new designs or design upgrade

- Equalizer
  - Option for new designs or design upgrade
  - Maxim MAX3784 (40” length, 6 mil, FR4, 5 Gbps)
Coupling

- Traces run in close proximity will couple
- Coupling is determined by geometry
  - trace separation, distance to ground(s) & parallel length
  - peaks at $\lambda/4$ and below $\lambda/4$ slope is 20 dB/decade

Notes:
1. Material FR4, $\varepsilon_r = 4.5$
2. Parallel length $= \lambda/4 = 1.39''$ at 1 GHz
3. Trace height $= 1.4$ mils
## Coupling Examples

### Strip-Line
- **11 mil width**
  - \( \lambda/4 \approx 1.39“ \)
  - | s   | Coupling |
    |-----|---------|
    | 0.011“ | 18 dB   |
    | 0.030“ | 35 dB   |

*Note:* Micro-Strip is more prone to coupling

### Micro-Strip
- **54 mil width**
  - \( \lambda/4 \approx 1.60“ \)
  - | s   | Coupling |
    |-----|---------|
    | 0.030“ | 18 dB   |
    | 0.054“ | 23 dB   |

*Notes:*
1. Copper: 1 oz, electrodeposited
2. FR4 dielectric constant: 4.50, height: 30 mils
3. F = 1.0 GHz
Mitigation of Coupling

- Separation of traces on same layer
- Reduce length of parallel run
- Run on separate non-adjacent layers
  - Ground plane in between
- Orthogonal runs on adjacent layers
- Run guard trace
  - Ground trace between lines
- Shield (for micro-strip)
- Dielectric height allocation

More Coupling

Less Coupling
**Differential Pairs**

- Lower Cross-talk, Lower Radiation
- Common mode noise rejection
- Reduces ground reference problems
- High dynamic range analog applications
  - Log Amplifiers
  - High Resolution ADC/DAC
- Low noise (small signal) analog applications
  - Transducers
- Critical High Speed Digital Applications
  - Low amplitude clocks
  - Low jitter requirements
Differential Pair Routing Options

- Geometry and spacing defined by artwork
- High differential impedance easily achievable
- Impedance reduced as “s” is reduced
- As “s” is increased, impedance approaches 2x single ended impedance
- Difficult to rout through fine pitch holes

- Geometry is effected by layer registration
- Low differential impedance easily achievable
- Easy to route, easy to maintain matched lengths
Differential Impedance Definitions

- **Single-Ended Impedance** ($Z_0$)
  Impedance on a single line with respect to ground when not coupled to another line
  \[ Z_0 = \sqrt{Z_{\text{Odd}}Z_{\text{Even}}} \]

- **Differential Impedance** ($Z_{\text{DIFF}}$)
  The impedance on one line with respect to the coupled line, when the lines are driven by equal and opposite signals

- **Odd Mode Impedance** ($Z_{\text{Odd}}$)
  Impedance on a single line with respect to ground when the other coupled line is driven by equal and opposite signals ($Z_{\text{DIFF}} = 2Z_{\text{Odd}}$)

- **Common Mode Impedance** ($Z_{\text{CM}}$)
  Impedance of the two lines combined with respect to ground

- **Even Mode Impedance** ($Z_{\text{Even}}$)
  The impedance on one line with respect to ground when the coupled line is driven by an equal and in-phase signal ($Z_{\text{Even}} = 2Z_{\text{CM}}$)
## Differential Impedance Examples

### Edge Coupled

![Edge Coupled Diagram](image)

<table>
<thead>
<tr>
<th>s</th>
<th>$Z_{Even}$</th>
<th>$Z_{Odd}$</th>
<th>$Z_0$</th>
<th>$Z_{Diff}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>49.4</td>
<td>49.4</td>
<td>49.4</td>
<td>98.8</td>
</tr>
<tr>
<td>25</td>
<td>50.9</td>
<td>47.9</td>
<td>49.4</td>
<td>95.8</td>
</tr>
<tr>
<td>10</td>
<td>56.4</td>
<td>41.9</td>
<td>48.6</td>
<td>83.8</td>
</tr>
</tbody>
</table>

### Broadside Coupled

![Broadside Coupled Diagram](image)

<table>
<thead>
<tr>
<th>s</th>
<th>$Z_{Even}$</th>
<th>$Z_{Odd}$</th>
<th>$Z_0$</th>
<th>$Z_{Diff}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>41.3</td>
<td>34.7</td>
<td>37.8</td>
<td>69.4</td>
</tr>
<tr>
<td>10</td>
<td>68.6</td>
<td>34.7</td>
<td>48.8</td>
<td>69.4</td>
</tr>
</tbody>
</table>
When coupled lines are close, most of the electric field is concentrated between the conductors
- Low ground currents
Field Intensity – 2

- As the coupled lines are separated and/or the ground planes are brought closer, less of the electric field is concentrated between the conductors, and more of the field is concentrated between the ground planes and the conductors.
As the coupled lines are separated and/or the ground planes are brought closer, less of the electric field is concentrated between the conductors, and more of the field is concentrated between the ground planes and the conductors.
Field Intensity - 4

- When coupled lines are far apart, most of the electric field is concentrated between the ground planes and the conductors
  - More ground return current
## PWB Pad and Trace Parameters

<table>
<thead>
<tr>
<th></th>
<th>10 mil trace</th>
<th>20 mil trace</th>
<th>100 mil trace</th>
<th>42 x 42 (≈ 0603)</th>
<th>60 x 60 (≈ 0805)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Capacitance</strong></td>
<td>2.2 pF/in</td>
<td>3.3 pF/in</td>
<td>11.6 pF/in</td>
<td>0.24 pF</td>
<td>0.45 pF</td>
</tr>
<tr>
<td><strong>Inductance</strong></td>
<td>9.9 nH/in</td>
<td>7.2 nH/in</td>
<td>2.4 nH/in</td>
<td>0.19 nH</td>
<td>0.21 nH</td>
</tr>
</tbody>
</table>

### Notes:
1. Copper: 1 oz, electrodeposited, strip-line.
2. FR4 dielectric constant: 4.50, loss tangent 0.025, height 10 mils.
Vias

♦ Needed to interconnect layers

♦ Minimize use
  - Introduce discontinuities (R, L, C)
  - “Choke-off” routing
  - Perforate Ground/Supply Planes

♦ Traditionally implemented with Plated Through Holes (PTHs)

♦ Consider Blind, Buried or Micro (4-6 mils) Vias
  - Escape routing of high density components
  - Additional processing cost can be offset by reduction in layers
Fine Pitch BGA (FG456) Package

Courtesy of Xilinx
Fine Pitch BGA (FG1156) Package

Courtesy of Xilinx
## Via Parameters

<table>
<thead>
<tr>
<th>Via Dia</th>
<th>10</th>
<th>12</th>
<th>15</th>
<th>25</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pad Dia</td>
<td>22</td>
<td>24</td>
<td>27</td>
<td>37</td>
</tr>
<tr>
<td>Anti-Pad Dia</td>
<td>30</td>
<td>32</td>
<td>35</td>
<td>45</td>
</tr>
<tr>
<td>Length: 60 Planes: 5</td>
<td>R</td>
<td>L</td>
<td>C</td>
<td>R</td>
</tr>
<tr>
<td>1.55</td>
<td>0.78</td>
<td>0.48</td>
<td>1.25</td>
<td>0.74</td>
</tr>
<tr>
<td>Length: 90 Planes: 7</td>
<td>R</td>
<td>L</td>
<td>C</td>
<td>R</td>
</tr>
<tr>
<td>2.3</td>
<td>1.33</td>
<td>0.66</td>
<td>1.88</td>
<td>1.24</td>
</tr>
</tbody>
</table>

**Notes:**
1. R in mΩ, L in nH, C in pF
2. Dimensions are in mils.
3. Planes are evenly spaced.
4. Via inductance can be approximated by:
   
   \[
   L = 5.08h \left[ \ln \left( \frac{4h}{d} \right) - 0.75 \right] \text{nH}
   \]

   h and d are in inches.
Source Terminations

- Driving waveform is reduced in half by series resistor at start of propagation
- Driving signal propagates at half amplitude to end of line
- At end reflection coefficient is +1
- Reduced peak current demands on driver
- Limited use with daisy-chained receivers
Destination Terminations

- Driving waveform propagates at full intensity over trace
- Reflections dampened by terminating resistor(s)
- Received voltage is equal to transmitting voltage (ignoring losses)
- Increased peak current demands on driver
- More applicable to daisy-chained receivers (first incident switching)
- Thevenin termination reduces steady-state drive current
“Intentional” Mismatch Example

♦ Five selectable sources
♦ Four destinations
♦ Modeled signal paths
  - CCA PWB
  - Back Plane PWB
  - Connectors
  - Driver
♦ Took advantage of relatively slow clock (30 MHz)
“Intentional” Mismatch Example

- Allow reflections to dissipate before clocking data (Clocks distributed point-to-point)
Power Distribution & Grounding
Power Distribution Purpose

- To distribute the supply voltages necessary to all components within the required regulation
- To provide a reliable reference (ground) for all circuitry
Supply Power Loss Budget

- Distribution loss contributes to supply voltage error delivered to CCA components

- Complete loss budget needs to be established, especially in high power applications
  - Power Supply Voltage Tolerance
  - Harnessing Loss
  - Connector Loss
  - Back-Plane Loss
  - PWB Loss

- Remote Sensing
  - Compensate for some losses
  - Location important
  - “Open Sense” protection
DC Loss Model
Power Distribution Considerations

♦ Dedicated Planes to Ground and Supply
  - Establishes low inductance distribution (when adjacent)
  - Parallel planes create distributed capacitance (typically not significant except for high $\varepsilon_r$ and/or thin material)
  - Gould (25 um, $\varepsilon_r = 3.5$)

♦ Through-holes perforate planes
  - Increases resistance

♦ Distributing localized supplies for analog
  - A dedicated voltage plane may not be practical or necessary
  - Rout power traces between ground planes as needed for isolation
**Plane Capacitance, Inductance, Resistance**

### Inductance

\[
L = \mu_0 h \frac{l}{w}
\]

\[
\mu_0 = 4\pi \times 10^{-7} \quad \frac{H}{m} = 0.32 \quad \frac{nH}{\text{inch}}
\]

### Capacitance

\[
C = \varepsilon_0 \varepsilon_r \frac{LW}{h} = \varepsilon_0 \varepsilon_r \frac{A_{\text{surface}}}{h}
\]

\[
\varepsilon_r = 225 \times 10^{-15} \quad \frac{F}{\text{in}}
\]

### Resistance

\[
R_{\text{DC}} = \rho \frac{l}{A_{\text{Cross-Sectional}}} = \rho \frac{l}{lw}
\]

\[
\rho = 0.679 \mu\Omega - \text{inch}
\]

Allowing \(l=w\) permits calculation of Resistance per Square.

\[
\frac{\text{Resistance}}{\text{Square}} = \rho \frac{1}{t} = (0.679 \mu\Omega - \text{in}) \frac{1}{0.0014} = 485 \mu\Omega / \text{Square}
\]

(For 1 ounce copper which is 0.0014" thick)

### FR4 Dielectric Thickness (mils) | Inductance (pH/square) | Capacitance (pF/inch²)
---|---|---
8 | 260 | 127
4 | 130 | 253
2 | 65 | 506

### Graphs

- **L&C as Function of Plane Separation**
- **Plane Capacitance**
- **Plane Inductance**

**Revision 4a**

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Capacitor Parameters

- Physical capacitors have parasitic elements that limit their ability to stabilize supply lines
- Equivalent series inductance (ESL)
- Equivalent Series Resistance (ESR)

Plots courtesy of Kemet

**FIGURE 5** Impedance versus Frequency X7R Dielectric

**FIGURE 7** X7R Capacitance & DF versus Applied AC/DC Voltages
### Capacitor Parameters

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
<th>Capacitance (uF)</th>
<th>ESL (nH)</th>
<th>ESR (Ω)</th>
<th>SRF (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C0603C103K5RAC, Kemet</td>
<td>EIA 0603</td>
<td>0.01</td>
<td>1.8</td>
<td>0.25</td>
<td>38</td>
</tr>
<tr>
<td>C0805C104K5RAC, Kemet</td>
<td>EIA 0805</td>
<td>0.10</td>
<td>1.9</td>
<td>0.10</td>
<td>12</td>
</tr>
<tr>
<td>T491B685K010AS, Kemet</td>
<td>EIA 3528-21</td>
<td>6.8</td>
<td>1.9</td>
<td>0.3</td>
<td>1.4</td>
</tr>
<tr>
<td>T494C476K010AS, Kemet</td>
<td>EIA 6032-28</td>
<td>47</td>
<td>2.2</td>
<td>0.2</td>
<td>0.5</td>
</tr>
</tbody>
</table>

\[
f_{SRF} = \frac{1}{2\pi \sqrt{LC}}
\]

*Self Resonant Frequency*

\[
Q = \frac{1}{DF} = \frac{X_C}{R} = \frac{1}{2\pi f \frac{C}{R}}
\]

*Quality Factor, Dissipation Factor*
Capacitor Guidelines

- Parasitic inductance is predominantly determined by package size
- Connect capacitor pads as directly as practical
- Don’t share cap vias
Notes:
1. Copper: 1 oz, electrodeposited, strip-line
2. FR4 dielectric constant: 4.50, loss tangent 0.025, height 10 mils
Decoupling Examples

- 100 MHz Logic Device, 100 mA to 150 mA step load change

- 6.8 uF, Ripple: 1 Vpp
- 6.8 uF + 0.1 uF, Ripple: 0.3 Vpp
- 6.8 uF + 0.1 uF + 0.01 uF, Ripple: 0.1 Vpp
- 6.8 uF + 0.1 uF + 0.01 uF w/ long traces, Ripple: 1.1 Vpp
Current Carrying Capability of PWB Traces

- Trace Cross section (w,t)
- Position of trace (outer layer, inner layer)
- Maximum acceptable temperature rise
- IPC-2221, Figure 6-4, can be used as general guideline
- Thermal modeling may be needed in critical applications
Trace Width Example

♦ Application
- Inner trace, 1 ounce, maximum fault current is 2 Amps
- Max CCA temp +90 °C, max PWB temp +150 °C, Margin 30 °C
- Allowable Temp rise = 150 – 90 – 30 = 30 °C

♦ Determine Cross Section from “C” is 56 sq mils
♦ Determine width from “B” to be 40 mils
References and Vendors
References

♦ IPC-2221 Generic Standard on Printed Board Design
♦ IPC-2222 Sectional Design Standard for Rigid Organic Printed Boards
♦ IPC-2223 Sectional Design Standard for Flexible Printed Boards
♦ IPC-4101 Specification for Base Materials for Rigid and Multi-Layer Printed Boards
♦ IPC-6012 Qualification and Performance Specification for Rigid Printed Boards
♦ IPC-SM-782 Surface Mount Design & Land Pattern Standard
♦ High Speed Digital Design, Howard W Johnson
♦ Even Mode Impedance, Polar Instruments, Application Note AP157
References (continued)

♦ Effect of Etch Factor on Printed Wiring, Steve Monroe, 11th Annual Regional Symposium on EMC
♦ Transmission Line Design Handbook, Brian C Wadell
♦ The Impact of PWB Construction on High-Speed Signals, Chad Morgan AMP/Tyco
♦ Transmission Line RAPIDESIGNER Operation and Applications Guide (AN-905) National Semiconductor
♦ PWB Design and Manufacturing Considerations for High Speed Digital Interconnection, Tom Buck, DDI
♦ Power Distribution System Design (XAPP623) Mark Alexander, Xilinx
♦ Surface Mount Capacitors, Kemet, Catalog F-3102G
Material Suppliers

- Park-Nelco, www.ParkNelco.com
- Polyclad, www.Polyclad.com
- Rogers, www.Rogers-Corp.com
PWB Fabricators

- DDI, www.DDIglobal.com
- Parlex, www.Parlex.com
Design Tools

- Ansoft
  [www.Ansoft.com](http://www.Ansoft.com)

- Cadance

- Eagleware
  [www.EagleWare.com](http://www.EagleWare.com)

- Polar Instruments
Viewgraphs Are Online

- Visit the IEEE Long Island Website
  www.IEEE.LI
- Click on Electromagnetic Compatibility Page
- Scroll down to the Viewgraphs
  Analog, RF & EMC Considerations in Printed Wiring Board Design

Thank You!